// VerilogA for SampleAndHold

`include "constants.vams"

`include "disciplines.vams"

module VerilogA\_SampleAndHold(clk,vin,vmin,vout);

parameter real vtrans=0.5;

parameter real delay = 0;

parameter real ttime = 1p;

parameter real clk\_threshold = 0.9; //vdd is 1.8v

input clk,vin,vmin;

output vout;

electrical vout,vin,vmin,clk;

real v;

analog begin

// Sampling Phase (+1 is for rising edge, -1 is for falling edge)

@(cross(V(clk) - clk\_threshold, -1))

v = V(vin) - V(vmin);

V(vout) <+ transition(v,delay,ttime);

end

endmodule